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## US UTILITY Patent Application





APPLICATION NO.	CONTIDDIOD					
a 09/955632	CONT/PRIOR	438	SUBCLASS	ART UNIT 2813	EXAMINER Y WAR	
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Kunai Parekh John Zahurak Phillip Wald

Capacitors, DRAM arrays, monolithic integrated circuits, and integrated circuits, and integrated circuits integrated circuits.

PTO-2040

## **ISSUING CLASSIFICATION** ORIGINAL CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK) INTERNATIONAL CLASSIFICATION HW PL 制造量的 中的 Continued on Issue Slip Inside File Jacket

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TERMINAL DISCLAIMER	4.3 6. 1	DRAWINGS		CLAIMS ALLOWED				
DIOCLAIMEN	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.			
The term of this patent	_			NOTICE OF ALLOWANCE MAILED				
subsequent to (date) has been disclaimed.	(Assistant Examiner) (Date)							
The term of this patent shall not extend beyond the expiration date					•			
of U.S Patent. No.	(Primary Examiner) (Date)			ISSUE FEE				
				Amount Due	Date Paid			
The terminal months of this patent have been disclaimed:		i	704 , F	ISSUE BATCH NUMBER				
機能の意味を含むしている。	(Legal Instrume	nts Examiner)	(Date)					
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